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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,626	03/29/2001	Andrew M. Lever	M4065.0432/P432	4425

7590

01/25/2002

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EXAMINER

NGUYEN, LINH M

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 01/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/819,626

Applicant(s)

LEVER, ANDREW M.

Examiner

Linh M. Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 July 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 5-7 and 9-22 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 8, 23 and 24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

Restriction to one of the following inventions is required under 35 U.S.C. 121:

- I. Claims 1-4, 8, 23-24, drawn to a charge pump circuit and a corresponding method of operation, classified in class 327, subclass 157.
- II. Claims 5-7, drawn to the structure of a CMOS logic circuit, classified in class 327, subclass 391.
- III. Claims 9-15, drawn to the structure of a lock loop circuit, classified in class 327, subclass 163.
- IV. Claims 16-22, drawn to a processor circuit, classified in class 711, subclass 5.

The inventions are distinct, each from the other because:

Inventions Group IV and each of Groups I, II, and III are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because claim 16 of Group IV is shown as an evidence that the configuration of the charge pump circuit of Group I, or that of group III, or that of the circuit portions containing transistors of different types of conductivity of Group II, is not believed to be required for patentability of Group IV. The subcombination has separate utility such as generating

rapid switching response as in Group I, or producing a fast current spike at its output as in Group II, or producing switching signals in accordance with a phase difference between the input signals as in Group III.

Inventions Group I, Group II, and Group III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, the Groups of inventions have separate utility such as (1) producing switching signals in accordance with a phase difference between the input signals as in Group III, (2) generating rapid switching response as in Group I, and (3) producing a fast current spike at its output as in Group II. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II or III or IV, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Michael Bergman on 01/09/2002, a provisional election was made without traverse to prosecute the invention of Group I, claims 1-4, 8, and 23-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 5-7, 9-22 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement might be traversed (37 CFR 1.143).

***Specification***

The disclosure is objected to because of the following informalities:

Page 8, line 14, change "13" to --B--.

Appropriate correction is required.

***Claim Objections/Minor Informalities***

Claim 1 is objected to because of the following informalities:

Claim 1, line 17, change "DOWN\N" to -- DOWN-- to correspond with Fig. 4.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in –

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or  
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-2, 4, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Arcus (U.S. Patent No. 6,124,741).

With respect to claim 1, Figure 9 of Arcus shows a charge pump circuit comprising 1) a first plurality of serially connected transistors [22,24] of a first conductivity type; 2) a second plurality of serially connected transistors [26,28] of a second conductivity type; 3) the first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors; 4) the interconnection of the first and second plurality of transistors providing an output [VCTL]; wherein a) a gate of one of the first plurality of transistors [22] is adapted to receive a DOWN pulse signal [PD], b) a gate of another one of the first plurality of transistors [24] is adapted to receive a DC bias signal [BIASP], c) a gate of one of the second plurality of transistors [28] is adapted to receive an UP pulse signal [PDB], and d) a gate of the other of the second plurality of transistors [26] is adapted to receive another DC bias signal [BIASN]; and 5) a first node [36] at the interconnection of the transistors of the first plurality of transistors being adapted to receive a DOWN pulse signal [Vpsrc], and a second node [38] at the interconnection of the transistors of the second plurality of transistors being adapted to receive an UP pulse signal [Vnsrc].

With respect to claim 2, Fig. 9 of Arcus discloses that the first plurality of transistors [22,24] are p-channel transistors, and the second plurality of transistors [26,28] are n-channel transistors.

With respect to claim 4, Fig. 9 of Arcus discloses that the first plurality of transistors [22, 24] is a pair of transistors, and the second plurality of transistors [26,28] is a pair of transistors.

With respect to claim 8, Fig. 9 of Arcus discloses a charge pump circuit comprising 1) a first plurality of serially connected transistors [22, 24] of a first conductivity type; 2) a second plurality of serially connected transistors [26,28] of a second conductivity type; 3) the first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors; 4) the interconnection of the first and second plurality of transistors providing an output [Vctl]; wherein a) a gate of one of the first plurality of transistors [22] is adapted to receive a first switching signal [PD], b) a gate of another one of the first plurality of transistors [24] is adapted to receive a DC bias signal [BIASP], c) a gate of one of the second plurality of transistors [28] is adapted to receive a second switching signal [PDB], and d) a gate of the other of the second plurality of transistors [26] is adapted to receive another DC bias signal [BIASN]; and 5) a first node [36] at the interconnection of the transistors of the first plurality of transistors being adapted to receive a complementary first switching signal [Vpsrc], and a second node [38] at the interconnection of the transistors of the second plurality of transistors being adapted to receive a complementary second switching signal [Vnsrc].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arcus (U.S. Patent No. 6,124,741).

With respect to claim 3, Arcus discloses all of the claimed limitations, as expressly recited in claim 1, except for a) a first capacitor circuit for coupling the DOWN pulse signal to the first node, and b) a second capacitor circuit for coupling the UP pulse signal to the second node. To configure in the charge pump circuit of Arcus a first capacitor for coupling the DOWN pulse signal to the first node, and a second capacitor circuit for coupling the UP pulse signal to the second node would have been obvious to one of ordinary skills in the art at the time of the invention since such an arrangement has been well-known in the art for its providing noise filtering for the DOWN and UP signals, and thus enhancing the turning ON/OFF process.

With respect to claims 23 and 24, Arcus discloses, in Fig. 9, a corresponding method of operating a charge pump comprising 1) switching a first switching transistor [22] in response to a first applied switching signal [PD] to affect an output at an output terminal; 2) switching a second switching transistor [24] in response to a second applied switching signal [PDB] to affect an output at the output terminal; and 3) biasing [BIASP,BIASN] the switching characteristics of said -first and second switching transistors with bias transistors [24,26] respectively serially connected to said first and second switching transistors. Arcus does not disclose the steps of a) capacitively coupling a complementary signal of the first applied switching signal to a connection between the first switching transistor and an associated bias transistor; and b) capacitively coupling a complementary signal of the second applied switching signal to



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a connection between the second switching transistor and an associated bias transistor. To perform these claimed steps, capacitive coupling is necessary. Consequently, to configure in the charge pump circuit of Arcus a first capacitor and second capacitor for respectively coupling the complementary signals of the first and second applied signals to the connections between the first and second transistors and respectively associated bias transistors would have been obvious to one of ordinary skills in the art at the time of the invention since such an arrangement has been well-known in the art for its providing noise filtering for the complementary signals and thus enhancing the turning ON/OFF process.

### ***Inquiry***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (703) 305-0414. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703) 308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-0142 for regular communications and for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

*Linh M. Nguyen*  
LmN

*Terry D. Cunningham*  
Terry D. Cunningham  
Primary Examiner